ABSTRACT OF THE DISCLOSURE

A clock divider circuit outputs a divided clock. A delay circuit is formed of at least one inverter to delay the divided clock to output a delayed, divided clock. An EXOR circuit receives the divided clock and the delayed, divided clock. A pulse width measurement circuit includes an integration circuit receiving a signal output from a logic circuit, and a Schmitt trigger circuit receiving a signal output from the integration circuit. Since the Schmitt trigger circuit's trigger potential is set to have a value corresponding to a predetermined pulse width, the pulse width measurement circuit outputs a signal asserted in response to a signal received from the logic circuit having a pulse with a width of no less than a predetermined value. A latch circuit latches a signal output from the pulse width measurement circuit.